High-frequency characterization of thermionic charge transport in silicon-on-insulator nanowire transistors

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We report on DC and microwave electrical transport measurements in silicon-on-insulator nano-transistors at low and room temperature. At low source-drain voltage, the DC current and radio frequency response show signs of conductance quantization. We attribute this to Coulomb blockade resulting from barriers formed at the spacer-gate interfaces. We show that at high bias transport occurs thermionically over the highest barrier: Transconductance traces obtained from microwave scattering-parameter measurements at liquid helium and room temperature are accurately fitted by a thermionic model. From the fits we deduce the ratio of gate capacitance and quantum capacitance, as well as the electron temperature. © *2014 AIP Publishing LLC*.
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Recent complementary metal-oxide semiconductor (CMOS) technology allows for the fabrication of silicon-on-insulator structures of nano-metric size. Depending on fabrication strategy, charge transport in these devices can be quasi-zero- or one-dimensional: Field-effect devices, based on narrow silicon channels with spacer regions surrounding the gate can exhibit single-electron-transistor (SET) characteristics,[1–3] whereas gate-all-around nanowires formed in Si fins show 1D behavior, e.g., conductance quantization due to subband formation.[4–6] Silicon nanowires on silicon-on-insulator (SOI) substrates have recently been shown to be promising candidates for future low-power and radio frequency (RF) applications.[6–9] The linearity of the RF response is improved due to the one-dimensional, ballistic charge transport in such devices, and the possibility to operate them in the so called quantum capacitance limit, where the gate voltage controls mainly the bands or levels in the transistor channel. Whether these requirements for RF linearity can also be met in devices that predominantly exhibit SET-like behaviour has not been studied extensively yet.

This Letter presents a study of the nature of electron transport in narrow channel CMOS silicon field-effect devices at low and high bias. They consist of a narrow Si channel in silicon-on-insulator substrate with a local top-gate and global back-gate. Spacer elements separate the source and drain electrodes from the top-gate, which in conjunction with surface roughness and remote charges in the gate stack induces two barriers in the potential landscape.[10] We show that at low temperature and low bias electron transport is governed by Coulomb blockade due to these barriers, observable directly, e.g., in the source-drain current as a function of bias and top-gate voltage at mK temperature. From microwave scattering-parameter measurements at low temperature we determine a different impact of the barriers depending on source-drain voltage: At low bias both barriers contribute, whereas at high bias transport occurs quasi-thermionically and only the highest of both barriers plays a role. Using a thermionic transport model, we are able to reproduce the device's transconductance and deduce the ratio of total capacitance and quantum capacitance as well as the electron temperature. Further microwave measurements show that the devices operate in the hot electron regime at high bias up to room temperature.

Devices were fabricated in fully depleted SOI substrate at LETI facilities. First the active regions were patterned by etching the SOI layer above the 145 nm buried oxide (BOX) forming undoped Si channels of thickness $t = 12$ nm. After short oxidation of the channel (0.8 nm) the gate stack is formed (1.9 nm HfSiON, 5 nm TiN and 50 nm polycrystalline silicon) and etched (see Fig. 1(e)). Silicon nitride spacers of length 11 nm were deposited on both sides of the gate and the source-drain contacts raised by epitaxial growth of Si (18 nm). Both source and drain were then highly doped by extension implantation and activation annealing. Figs. 1(a) and 1(b) show, a sketch and a TEM micrograph of a typical device. Similar to Ref. 2 the devices have a non-overlap profile due to the Si_3N_4 spacers. The doping gradient under the spacers together with surface roughness and remote charges in the gate stack induce potential barriers as sketched in Fig. 1(c). In a last step the devices were silicided (NiPtSi). All devices presented in this Letter are embedded in a 50Ω adapted coplanar wave guide for RF measurements (see Fig. 1(d)). Gate lengths L_g and channel widths W of devices present in this Letter are shown in Table I.

DC and RF probe station measurements were carried out at room temperature and liquid helium temperature in a *Janis* variable temperature probe station. The RF response was probed with a vector network analyzer at frequencies $f \leq 20$ GHz: After a short-open-load-through calibration, we obtained the scattering parameters $S_{ij}(\omega)$, $i,j = 1,2$ for each pair of gate voltages and converted them to admittance parameters $Y_{i,j}(\omega)$.[11] The conversion is favourable since

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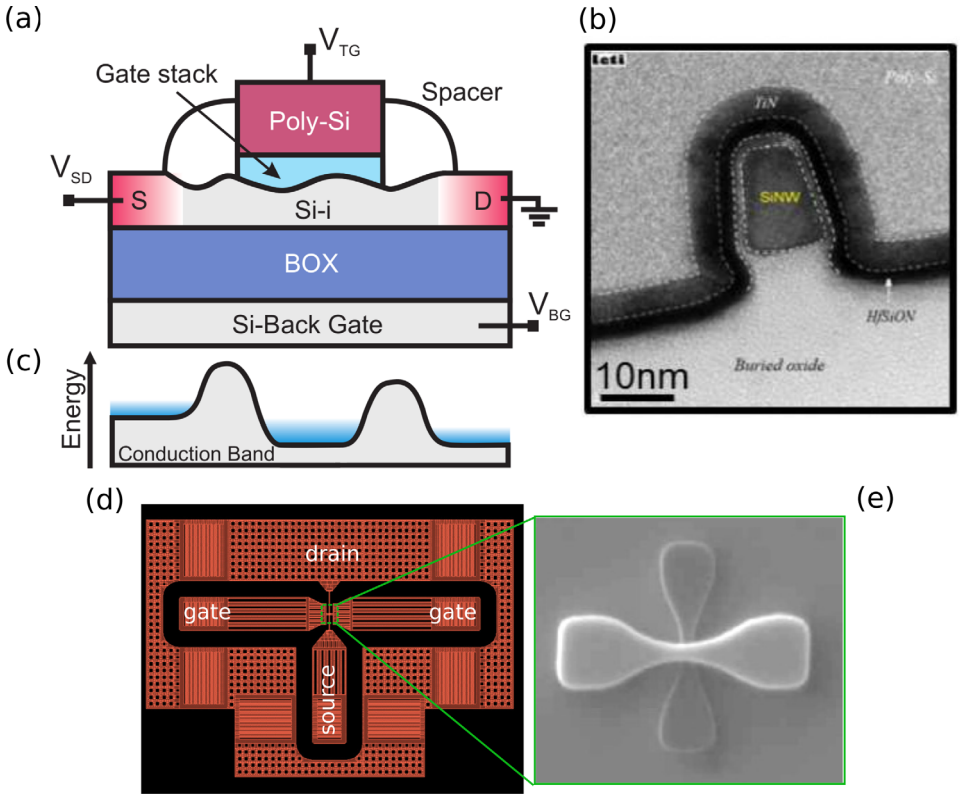

FIG. 1. Device design and potential profile. (a) Sketch of device cross-section. From bottom to top: Undoped Si handle wafer (grey), 145 nm buried oxide (blue), undoped Si channel of thickness 11 nm (grey, width $W = 10 - 60$ nm) and thin dielectric stack (light blue, 0.8 nm SiO_2, 2.3 nm HfSiON) separating top-gate from channel (red, gate lengths $L = 44$ nm, 64 nm, and 114 nm). Highly doped source and drain separated from gate by SiN spacers (white). (b) Transmission electron micrograph of typical device cross-section perpendicular to the channel. (c) Sketch of energy profile along the channel. Potential barriers form at spacer-gate interface. (d) High frequency chip design: Devices are embedded in 50 Ω adapted coplanar wave-guide with surrounding ground plane. (e) Scanning electron micrograph of highlighted region in (d) during fabrication.

parasitic, parallel elements can then simply be subtracted.[12] We use the device's off-state as dummy signal and obtain the de-embedded admittance $Y_{DUT}(\omega, V_{bg}, V_{tg}) = Y_{exp.}(\omega, V_{bg}, V_{tg}) - Y_{off}(\omega, V_{bg}, V_{tg} \ll V_{th})$, where V_{th} is the threshold voltage, V_{tg} the top-gate, and V_{bg} the back-gate voltage. Note that in the following the subscript *DUT* is omitted and Y_{ij} refers to the de-embedded admittance signal. DC traces are recorded simultaneously with the RF measurements.

In Fig. 2 we present first of all the DC current I_{ds} of device RFM1-2 ($W = 30$ nm, $L_g = 44$ nm) at $T_0 = 300$ K as a function of top-gate voltage for various back-gate voltages. The device shows a good transistor behavior with off-state current in the pA region for $V_{ds} = 0.5$ V and a subthreshold slope $S \simeq 64 - 69$ mV/dec (see Fig. 2), close to the theoretical limit of $k_B T ln(10)/q \simeq 60$ mV/dec for thermally activated transport at $T = 300$ K.[13] Here, k_B is the Boltzmann constant and q the electron charge. As previously reported in Ref. 2 the threshold voltage V_{tg} shifts with back-gate voltage. We turn now to characterizing the nature of charge transport in our devices. As described in the introduction of this Letter, charge transport through a narrow silicon channel can in general occur via one-dimensional channels[6] or through the levels of a single-electron-transistor-like structure.[2] In order to discriminate between the two mechanisms, we have carried out DC measurements in a dilution fridge setup at $T_0 = 30$ mK and RF probe station measurements at $T_0 = 5$ K.

TABLE I. Device dimensions.

Device	L_g (nm)	W (nm)	*Device*	L_g (nm)	W (nm)
RFM2-1	44	10	*RFM4-3a*	64	30
RFM1-2	44	30	*RFM4-3b*	64	30
RFM1-4	64	10	*RFM3-1*	114	10

Fig. 3(a) is a colorscale plot of the current I_{ds} in sample RFM1-4 just below the turn-on voltage of the transistor at $T_0 = 30$ mK. Clear Coulomb diamonds are visible, indicating the presence of two barriers and subsequent conductance quantization as depicted in Fig. 1(c) and the inset to Fig. 3(a). Fig. 3(b) shows the transconductance g_m of devices RFM4-3, RFM3-1, and RFM2-1 at low bias and $T_0 = 5$ K and 30 mK, respectively. The DC transconductance is calculated from the DC current as $g_m^{DC} = \partial I_{ds}/\partial V_{tg}$. At RF it can directly be read from the forward admittance as $g_m^{RF} = \Re(Y_{21})$. Similar to the device of Fig. 3(a), RFM4-3a and RFM4-3b show Coulomb blockade at low V_{ds} with a charging energy of about 15 meV (not shown here). The DC transconductance reflects this, as can be seen from the oscillations of g_m at $V_{ds} = 25$ mV in Fig. 3(b). In addition, the DC transconductance remains flat below threshold. Above

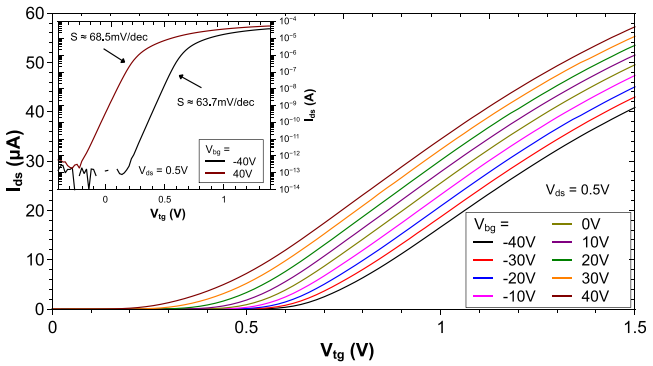

FIG. 2. Device RFM1-2 at $T_0 = 300$ K. Main panel: Source-drain current I_{ds} as function of top-gate voltage V_{tg} at high source-drain bias for back-gate voltages $V_{bg} = -40$ V - 40 V. Inset: $log_{10}(I_{ds})$ as function of V_{tg} at $V_{bg} = \pm 40$ V. The subthreshold swing S is calculated from the inverse of $d(\log_{10} I_{ds})/dV_{tg}$.

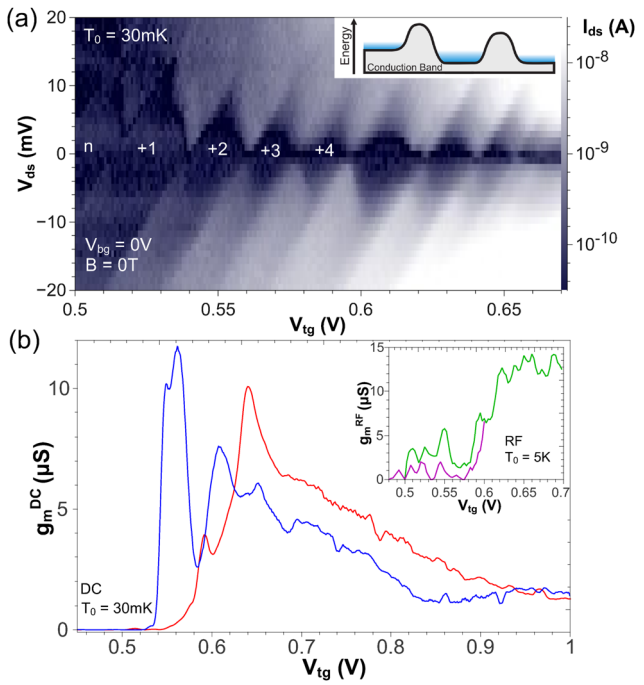

FIG. 3. (a) Source-drain current I_{ds} as function of V_{ds} and V_{tg} in device RFM1-4 ($W = 10\,\text{nm}$, $L_g = 64\,\text{nm}$) at $T_0 = 30$ mK and $V_{bg} = 0\,\text{V}$. Coulomb diamonds are clearly visible in the V_{tg} range just below turn-on. Inset: Sketch of the potential landscape due to the barriers at the spacer-gate interfaces at low bias. (b) Main panel: DC transconductance $g_m^{DC}(V_{tg}) = \partial I_{ds}/\partial V_{tg}$ in devices RFM4-3a (blue) and RFM4-3b (red) at $T_0 = 30$ mK and $V_{ds} = 25\,\text{mV}$. Inset: RF transconductance $g_m^{RF} = \Re(Y_{21})$ of devices RFM3-1 (green) and RFM2-1 (purple) at $T_0 = 5\,\text{K}$ and $V_{ds} = 5\,\text{mV}$ (RFM3-1) and $10\,\text{mV}$ (RFM2-1), respectively.

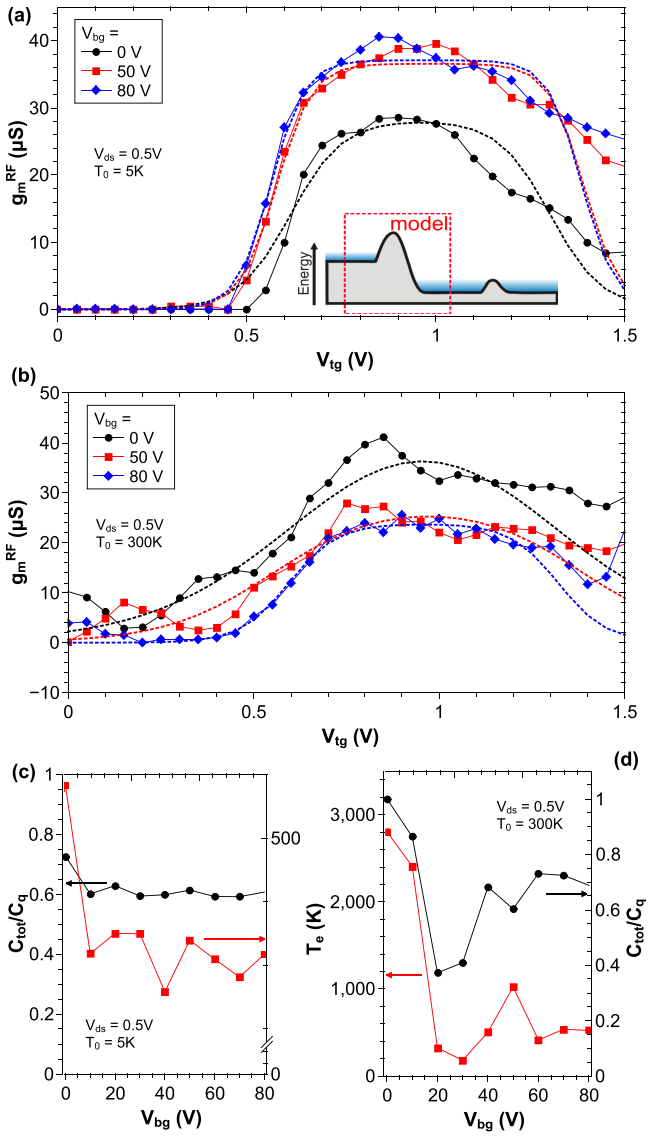

FIG. 4. Device RFM2-1 (a) RF transconductance at low temperature and high bias. Symbols show the measured values at three different back-gate voltages. Dashed lines are fits to the data following the thermionic model of Eq. (1). The high bias potential landscape is sketched as inset. (b) RF transconductance at room temperature and high bias. As in the $T = 5\,\text{K}$ case data can be accurately fitted by the thermionic model. (c) and (d) Electron temperature T_e and capacitance ratio β at $T_0 = 5\,\text{K}$ and $300\,\text{K}$ obtained from the thermionic fits in (a) and (b).

threshold we observe two g_m^{DC} peaks and a steady decline thereafter. The RF counterparts of RFM3-1 and RFM2-1 were obtained at $T_0 = 5\,\text{K}$ and $V_{ds} = 5\,\text{mV}$ and $10\,\text{mV}$, respectively. Consequently, these traces exhibit several peaks below threshold as function of V_{tg} with a gate spacing of $\Delta V_{tg} \simeq 15 - 22\,\text{mV}$ for RFM2-1 (purple). For the device of longest gate length, RFM3-1 (green), peaks below threshold are less pronounced, but prevail beyond threshold, similar to g_m^{DC} of devices RFM4-3a and b. We attribute the additional small variations, e.g., at $V_{tg} \simeq 0.6\,\text{V}$, to increased disorder in the device. Overall, we infer that low bias transport is governed by barriers formed at the spacer-gate interfaces. Their effect manifests in both DC and RF measurements.

The picture changes when the source-drain bias is raised to higher values: Fig. 4(a) shows the transconductance extracted from low temperature RF scattering-parameter measurements in device RFM2-1. Contrary to the low bias case of Fig. 3(b), g_m now shows only one broad peak as function of V_{tg}. Owing to the high V_{ds}, i.e., large potential drop between source and drain, transport is now dominated by only one barrier. In the following, we fit data by a simple 1D nanotransistor model derived from material independent Landauer-Buettiker transport theory.[14,15] The derivation of the model is outlined in Ref. 16. Here, the transistor is described as a 1D channel with one classical barrier between the leads. A corresponding potential landscape is shown as inset of Fig. 4(a). The model takes into account a potential as highlighted in red. Only electrons with energies high enough to clear the barrier of height Φ contribute to the charge transport in this model, i.e., we assume a transmission $D(\epsilon) \simeq 0$ for $\epsilon < \Phi$ and $D(\epsilon) \lesssim 1$ for $\epsilon \geq \Phi$, in accord with estimates for this particular device structure.[17] Transport over the barrier is thus thermionic and one can derive the corresponding transconductance[16]

$$g_m = \alpha\beta \frac{4e^2}{h} [f_s(\Phi) - f_d(\Phi)], \tag{1}$$

where $\beta = C_g/C_q$. $C_g = (C_{ox}^{-1} + C_q^{-1})^{-1}$ and C_q are the total gate and the quantum capacitance,[18] respectively; α is an additional factor accounting for residual diffusive charge transport over the barrier and the factor 4 accounts for spin and valley degeneracy. The contacts are modelled by the Fermi distributions $f_s(\epsilon, T_e)$ and $f_d(\epsilon, T_e) = f_s(\epsilon + eV_{ds}, T_e)$,

where T_e is the electron temperature. All three parameters, α, β, and T_e, depend on source-drain voltage and back-gate bias. Assuming that the barrier height is controlled by V_{tg}, i.e., $\Phi(V_{tg}) = const. - qV_{tg}\beta$, as well as $\epsilon \ll \Phi$[16] and using α, β, and T_e as fitting parameters, we obtain the dashed lines shown in Figs. 4(a) and 4(b). The good agreement between data and fit—performed for each V_{bg}—shows that transport is dominated by only the highest barrier in the high bias regime and can be regarded as quasi one-dimensional. At low temperature the transconductance peak is more pronounced than at room temperature and we find from the fits that the device works in the hot electron regime: The electron temperature T_e, shown in Fig. 4(c) as function of V_{bg}, is much higher than the substrate temperature $T_0 = 5$ K. Fig. 4(c) also presents the extracted ratio β of total gate to quantum capacitance. On average $\beta \simeq 0.6$, i.e., $C_q \simeq C_{ox}/2$. The device hence operates in between the classical, charge controlled limit $(\beta \to 0)$ and the quantum capacitance limit $(\beta \to 1)$.[9] Similar to the RF transconductance, one can obtain the total gate capacitance from RF Y-parameter measurements as $Y_{11}(\omega) = j\omega(C_{gs} + C_{gd})$. We find $C_{tot} \simeq 600 - 50$ aF for $V_{bg} = 0$–80 V. Residual diffusive transport remains moderate with an average "ballisticity" factor $\alpha \approx 0.38$ (not shown here). At room temperature, we obtain a noisier RF response and thus larger uncertainty in the fitting procedure. Data can still be modelled by Eq. (1), i.e., transport is still thermionic. On average, the electron temperature remains at a similar level as in the low temperature measurements (see Fig. 4(d)), as does the capacitance ratio β. Residual diffusive transport however increases at room temperature and we now obtain on average $\alpha \approx 0.3$ (not shown here).

In conclusion, we have studied the nature of charge transport at low and high bias in narrow channel SOI field-effect devices. We show that at low bias transport is governed by barriers emerging in the undoped region under the spacer elements, whereas at high bias transport occurs quasi-one-dimensional over the highest barrier. In the latter case the device's behaviour can be described with a thermionic transport theory and we accurately model the device transconductance. The devices operate in the thermionic transport regime from liquid helium to room temperature.

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