

Single Carbon Nanotube Transistor at GHz Frequency

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ABSTRACT

We report on microwave operation of top-gated single carbon nanotube transistors. From transmission measurements in the 0.1–1.6 GHz range, we deduce device transconductance g_m and gate–nanotube capacitance C_g of micro- and nanometric devices. A large and frequency-independent $g_m \sim 20 \mu\text{S}$ is observed on short devices, which meets the best dc results. The capacitance per unit gate length of 60 aF/ μm is typical of top gates on a conventional oxide with $\epsilon \sim 10$. This value is a factor of 3–5 below the nanotube quantum capacitance which, according to recent simulations, favors high transit frequencies $f_T = g_m/2\pi C_g$. For our smallest devices, we find a large $f_T \sim 50$ GHz with no evidence of saturation in length dependence.

Carbon nanotube field effect transistors (CNT-FETs) are very attractive as ultimate, quantum limited devices. In particular, ballistic transistors have been predicted to operate in the sub-THz range.^{1,2} Experimentally, a state-of-the-art cutoff frequency of 30 GHz has been reached in a low impedance multi-nanotube device,³ whereas 8 GHz was achieved with a multigate single nanotube transistor.⁴ Indirect evidence of microwave operation was also obtained in experiments based on mixing effects or channel conductance measurement in single nanotubes.^{5–9}

The extraordinary performances of nanotubes as molecular field effect transistors rely on a series of unique properties. High-mobility “p-doped” single-walled nanotubes can be obtained by CVD growth, with a semiconducting gap of $\Delta \sim 0.5$ –1 eV (diameter 1–2 nm).¹⁰ Low Schottky barrier contacts, with Pd metallization, and quasi-ballistic transport result in a channel resistance R_{ds} approaching the quantum limit, $h/4e^2 = 6.5$ k Ω for a four-mode single-walled nanotube.¹¹ High saturation currents, limited by optical phonon emission, allow large biases, $I_{ds} \sim 20 \mu\text{A}$ at $V_{ds} \gtrsim 1$ V, in short nanotubes.^{12,13} The above numbers and the good

gate coupling explain the large transconductances, $g_m \sim I_{ds}/\Delta \gtrsim 10 \mu\text{S}$, observed in dc experiments.¹ In the ac, an intrinsic limitation is given by the transit frequency $f_T = g_m/2\pi C_g$, where C_g is the gate–nanotube capacitance. Here, $C_g = C_{\text{geo}}C_Q/(C_{\text{geo}} + C_Q)$ is the series combination of the quantum and geometrical capacitances, C_Q and C_{geo} . An ultrathin oxide coating in CNT-FETs allows approach to the quantum limit with a capacitance per unit gate length of l_g , $C_{\text{geo}}/l_g > C_Q/l_g = 4e^2/hv_F \sim 400$ aF/ μm for $v_F \sim 4 \times 10^5$ m/s, a typical value for semiconducting NTs.¹⁴

Beside basic interest for quantum limited nanodevices, single nanotube transistors offer new opportunities for fast charge detection due to the unique combination of short time response and high charge sensitivity. At present, charge counting experiments performed in nanotube or semiconducting quantum dots use either single electron transistors^{15,16} or quantum point contact detectors,¹⁷ which operate on microsecond time scales. The high sensitivity of the NT-FET has been demonstrated recently by monitoring tunneling events between the nanotube and a nearby gold particle¹⁸ at the dc limit. Performing such experiments with quantum dots at nanosecond time scales would allow one to extend charge counting in the coherent regime relevant for full quantum electronics.¹⁹ Given the shot noise limitation of a nanotube detector of bandwidth $1/\tau = 1$ ns⁻¹, overestimated by the Poissonian value of $\sqrt{I_{ds}\tau/e} = 250$ electrons for $I_{ds} \sim 10$

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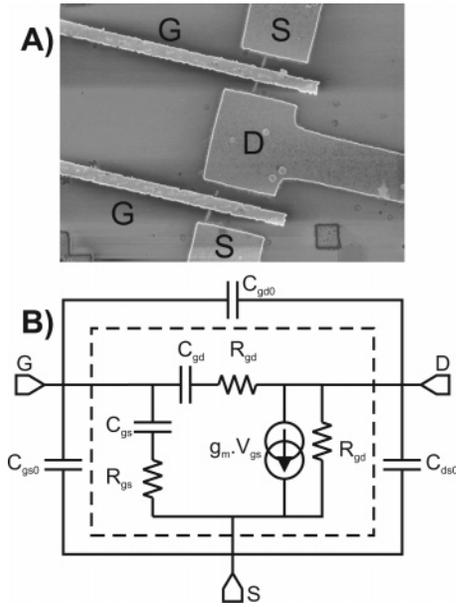


Figure 1. Panel A: scanning electron microscope image of a single carbon nanotube double-gate transistor. The gate length is 300 nm. Panel B: small-signal-equivalent circuit of the carbon nanotube transistor. Extrinsic components are displayed outside of the dashed rectangle. Notations are explained in the text.

μA , single charge resolution requires a charge gain of $g_m \tau / C_g \geq 250$ or, equivalently, a transit frequency of $f_T = g_m / 2\pi C_g \geq 40$ GHz.

In this letter, we demonstrate room-temperature broadband GHz operation ($f = 0.1\text{--}1.6\text{GHz}$) of nanotransistors made of a single carbon nanotube, with $l_g = 0.3$ and $3 \mu\text{m}$ (channel lengths 1 and $3.5 \mu\text{m}$, respectively). Our main results are the high $g_m \sim 10\text{--}20 \mu\text{S}$ in short tubes and the scaling $C_g \propto l_g$. From the latter, we deduce $C_g/l_g \sim 60 \text{ aF}/\mu\text{m}$, in accordance with previous low-frequency determinations,²⁰ and $f_T \sim 50$ GHz for our $l_g = 300$ nm devices.

Double-gate carbon nanotube transistors were fabricated by e-beam lithography in a coplanar strip-line geometry, with two symmetric top gates (see Figure 1), on oxidized high-resistivity silicon substrates (resistivity 3–5 k Ω .cm). Nanotubes were synthesized from nano-patterned catalyst pads using a standard CVD recipe. Palladium contact evaporation was followed by multistep oxidation of thin aluminum, for a total oxide thickness of ≈ 6 nm, and finally gold-gate deposition. This process provides full oxidation of Al into Al₂O₃ with $\epsilon \approx 9.8$. From sample geometry and dielectric constants, we estimated $C_{\text{geo}}/l_g \sim 100 \text{ aF}/\mu\text{m}$.

Devices were characterized in a standard S -parameter measurement using a rf probe station and a network analyzer. Attenuators (–6 and –10 dB), followed by bias tees, were mounted directly at the input and output ports of the station to minimize standing waves in the $Z_0 = 50 \Omega$ cables due to large impedance mismatch, $R_{\text{ds}}/Z_0 \sim 300$. To compensate for small voltage gain, $Z_0 g_m \sim 10^{-3}$, output signals were amplified by two 0.1–2 GHz bandwidth low noise amplifiers in series. As a consequence, the S -parameter measurement was restricted to the transmission coefficient $S_{21}(V_{\text{ds}}, V_g)$, which in turn could be accurately calibrated.

Data reduction and analysis are based on the standard equivalent circuit of Figure 1B. Extrinsic elements, $C_{\text{gs}0} \sim C_{\text{ds}0} \sim 10\text{--}20$ fF, estimated from independent reflection measurements, and $C_{\text{gd}0} \sim 2$ fF measured as explained below, were minimized by the coplanar sample design. The gate capacitance $C_g = C_{\text{gd}} + C_{\text{gs}}$ was split into gate–drain C_{gd} and gate–source C_{gs} contributions. These are associated with charge relaxation resistances R_{gd} and R_{gs} . We have $R_{\text{gd}} \gg 1/C_{\text{gd}}\omega$ in the OFF state ($V_g \geq 1$ V) and $R_{\text{gd}} \ll 1/C_{\text{gd}}\omega$ in the ON state ($V_g \leq 0$ V). Considering that $Z_0 C_{\text{gs}0}\omega \sim 10^{-2}$, $Z_0 C_{\text{gd}0}\omega \sim 10^{-3}$, and $Z_0 g_m \sim 10^{-3}$ in the low-frequency range of $\omega/2\pi \leq 1.6$ GHz of our experiment, we obtained

$$S_{21} = S_{21}^0 + S_{21}^p(V_g) + S_{21}^a(V_{\text{ds}}, V_g)$$

with

$$S_{21}^0 \approx j 2Z_0\omega C_{\text{gd}0} \quad (1)$$

$$S_{21}^p \approx j 2Z_0\omega C_{\text{gd}}/(1 + j\omega C_{\text{gd}}R_{\text{gd}}) \quad (2)$$

$$S_{21}^a \approx -2Z_0g_m + \Delta S_{21}^p(V_{\text{ds}}) \quad (3)$$

being, respectively, the background transmission amplitude in the pinched state, the passive contribution at the onset of channel conduction in the zero bias state, and the active contribution under bias. Note that $\Delta S_{21}^p = S_{21}^p(V_{\text{ds}}) - S_{21}^p(0)$ constitutes the imaginary part of S_{21}^a .

In order to check the validity of our analysis, we first consider the case of long FETs ($l_g = 3 \mu\text{m}$) where gate capacitance contributions are easily resolved. Typical data are exhibited in Figure 2. The inset of Figure 2A shows both quadratures of the background transmission $S_{21}^0(f)$. From the slope of $\mathcal{F}(S_{21}^0)(f)$ and eq 1, we deduce the small $C_{\text{gd}0} \sim 1.5$ fF. Subtraction of this contribution, keeping zero bias conditions, gives the V_g -dependent passive contribution $S_{21}^p(f)$ shown in (Figure 2A,B). In the ON state, $\mathcal{F}(S_{21}^p)$ has a linear frequency dependence, whose slope is plotted in Figure 2C as a function of V_g . The pinch-off transition appears here as a strong discontinuity associated with the divergence of the charge relaxation resistance R_{gd} . From the step amplitude and by using eq 2, we deduce $C_{\text{gd}} \approx 170$ aF. This value is very representative of the five long samples which we have measured with an average of 160 aF and a standard deviation of 50 aF. A small monotonic dependence in $\mathcal{R}(S_{21}^p)(V_g)$ (Figure 2A) is also observed, which is possibly due to a residual substrate conduction, not taken into account in our analysis.

The active contribution (Figure 2D,E) is obtained from the bias dependence of $S_{21}(f)$ at constant V_g . The in-phase signal $\mathcal{R}(S_{21}^a)(f)$ is prominent and almost frequency-independent. Slow frequency oscillations are reminiscent of calibration imperfections. Averaging $\mathcal{R}(S_{21}^a)$ over 0.2–1.6 GHz gives, according to eq 3, the transconductance as a function of V_g shown in Figure 2F. It has a maximum of $g_m \lesssim 3 \mu\text{S}$ close to the maximum observed at the dc ON–OFF transition. Representative values are $g_m \lesssim 1\text{--}4 \mu\text{S}$. The small negative part, $\mathcal{F}(S_{21}^a) \sim -\mathcal{F}(S_{21}^p)$ in Figure 2E, is a

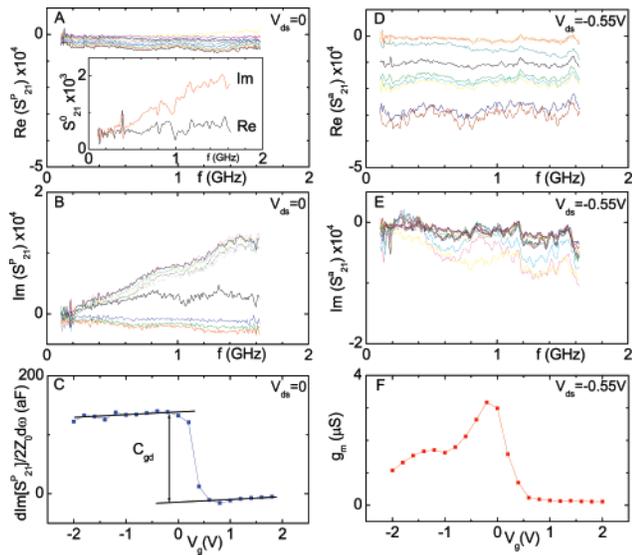


Figure 2. A 3 μm gate transistor. Transmission amplitude S_{21} as function of frequency. Background contribution (inset of panel A), passive zero bias (panels A and B), and active-biased (panels D and E) contributions. Panels A and D (respectively, B and E) have the same scales for direct data comparison. Lines correspond to $V_g = -2$ –2 V with an increment of 0.4 V. Panel C gives the slope $(d\text{Re}[S_{21}^p(\omega)]/d\omega)$ as function of gate voltage. It shows a discontinuity at the opening of the channel conductance associated with the gate–drain capacitance. Panel F shows the device transconductance.

capacitive contribution due to a shift of the pinch-off under bias. Altogether, these measurements show that one can quantitatively analyze the dynamical properties of a single nanotube transistor. With $g_m \sim 1.5 \mu\text{S}$ and $C_g \sim 170 \text{ aF}$ (per gate finger), the transit frequency of the 3 μm device of Figure 2 is $f_T \sim 1.5 \text{ GHz}$.

For short NT-FETs ($l_g = 300 \text{ nm}$ in Figure 1), we observe a smaller C_{gd} and larger g_m due to smaller channel resistance. The example shown in Figure 3 represents a new state-of-the-art for rf operation, with a maximum of $g_m(V_g) \geq 20 \mu\text{S}$ (double-gate fingers). Gate–drain capacitance is $C_{gd} \approx 35 \text{ aF}$ (standard deviation of 25 aF). Average values for the six short NT-FETs measured are $g_m \approx 12 \mu\text{S}$ and $C_{gd} \approx 35 \text{ aF}$ (double-gate fingers). As seen in the dc characteristics in the inset of Figures 3B, hysteresis is observed in these measurements, which has been omitted elsewhere for clarity. Comparing our data for the 300 nm and 3 μm devices shows that, within experimental uncertainty, C_{gd} scales with l_g . Assuming symmetric distribution of gate–drain and gate–source capacitances at zero bias, we obtain $C_g/l_g \approx 2C_{gd}/l_g \approx 60 \text{ aF}/\mu\text{m}$. With $g_m \sim 10 \mu\text{S}$ and $C_g < 30 \text{ aF}$ (per gate finger), the transit frequency of the 300 nm device of Figure 3 is $f_T \geq 50 \text{ GHz}$.

These measurements show that NT-FET performances do improve drastically upon gate size reduction down to the nanometric scale (factor of 30 in f_T for a factor of 10 in size). We now discuss possible routes for improvements. The first one is to increase g_m by reducing the access resistance due to the ungated NT sections at the drain and source (see Figure 1A). This effect is significant on devices using deposited CNTs; it is minimized with in situ CVD-grown NTs which

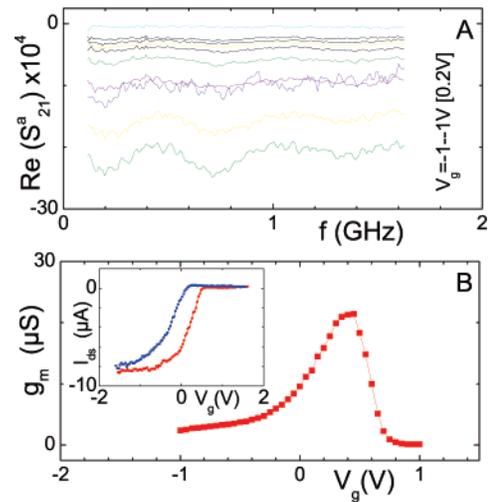


Figure 3. Characterization of a 300 nm gate transistor. Transmission amplitude of the active contribution (panel A) and transconductance (panel B). Inset shows hysteresis in the dc characteristics as V_g is swept.

are naturally p-doped in the absence of gating. Actually, ungated regions are needed to reduce direct gate–drain/source capacitive coupling. Our values for gate capacitance are close to the estimate for the geometrical contribution and in accordance with previous low-frequency measurements in similar top-gated devices.²⁰ They are still smaller than the above numbers for the quantum capacitance. One may wonder whether better performance could be achieved by working closer to the quantum limit in using high- κ and/or thinner oxides. This would improve gate coupling but, at the same time, slow down electron dynamics due to the screening of electronic interactions, as discussed in ref 21. In the absence of experimental data and the theoretical model, we shall rely on recent numerical simulations showing that the transit frequency is maximized for $C_Q \geq 3$ –5 $\times C_{geo}$.¹⁴ This condition is close to our experimental realization. The most promising route is further size reduction below 100 nm as we have not observed evidence for saturation down to 300 nm. Finally, noise performance remains to be characterized, in particular, the conditions for shot-noise limited resolution.

In conclusion, we have demonstrated high-transconductance SWNT-FET properties up to 1.6 GHz. We observe that high sensitivity is preserved and that gate capacitance scales with gate length down to 300 nm. Transit frequencies as high as 50 GHz have been inferred, indicating that nanotube FETs are promising fast sensors.

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