Implementation of a combined charge-phase quantum bit in a superconducting circuit

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Abstract

We discuss a qubit circuit based on the single Cooper-pair transistor (which consists of two ultrasmall Josephson junctions in series) connected in parallel with a large Josephson junction. The switching of this junction out of its zero-voltage state is used to readout the qubit. We report measurements of the discriminating power of the readout process, and we discuss its back-action on the qubit. © 2002 Elsevier Science B.V. All rights reserved.

1. Introduction

The recently proposed quantum computing schemes are based on the controlled evolution of a set of two-level systems, called qubits (see Ref. [1] for a review). Suitable qubits should have a quantum coherence time much longer than the duration of an elementary operation, and be measurable when necessary. Among the various systems proposed for implementing qubits, nano-fabricated solid-state circuits are particularly attractive because they are more easily scalable. The presently most investigated solid-state qubits are the "single Cooper-pair box" [2], in which Rabi precession of a coherent superposition of the qubit states has been demonstrated [3], and the "flux box" [4]. In the Cooper-pair box, the qubit states

are spanned by discrete charge states of a superconducting small metallic island, and are controlled by the gate charge coupled to the island. In the flux box, the qubit states are spanned by flux states of a small superconducting loop, and are controlled by the flux threading the loop. Whereas some simple qubit manipulations have already been realised in these systems, no readout of a single qubit has yet been achieved. In the case of the Cooper-pair box, the measurement of the island potential either by means of a radio-frequency single electron transistor [5] or of a single Cooper-pair transistor [6], is nevertheless believed to reach a sensitivity sufficient for such a "single-shot" readout. In this paper, we discuss a qubit circuit which is controlled both by a charge and by a phase. In this combined charge-phase qubit, qubit control is performed by acting on the gate charge like in the Cooper-pair box, but the measured quantity is a supercurrent, like in the flux box. The main interest of this Q–δ design is to provide (i) a good immunity respectively to the

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offset charge noise, which is presently considered as the major source of decoherence in charging devices, (ii) a good decoupling from the measuring system when readout is not active, and (iii) a fast pulsed readout. We explain below the operating principle of this Q–δ qubit, and we report first measurements of the readout system resolution.

2. Operating principle of a combined Q–δ qubit based on the single Cooper-pair transistor

The qubit circuit we consider (see Fig. 1a) is based on the single Cooper-pair transistor (SCPT) [7], which consists of two nominally identical ultrasmall junctions in series. When a phase difference δ is imposed across the transistor by means of

Fig. 1. (a) Schematic circuit of a Q–δ qubit based on a superconducting SCPT in a flux-biased loop; (b) full circuit with a readout Josephson junction, and a bias-current source with admittance $Y(\omega)$. Readout is based on the dependence of the critical current of the system on the qubit state. (c) Effective admittance implemented in the present experiment. An on-chip capacitor $C \approx 1$ pF is connected in parallel with an 500 Ω–10 pF RC-series circuit made with surface mounted components.

a small superconducting loop threaded by an applied flux, this device is equivalent to a single Cooper-pair box with an effective Josephson coupling $E_J = 2E_J^0 \cos(\delta/2)$, where E_J^0 is the Josephson energy of each junction with critical current $i_C = E_J^0/\varphi_0$ ($\varphi_0 = \hbar/2e$). The hamiltonian of the transistor depends both on the phase δ and on the gate charge $n_g = C_g U/2e$, and can be written as:

$$H = -2E_J^0 \cos(\delta/2) \cos\widehat{\theta} + E_C(\widehat{n} - n_g)^2. \qquad (1)$$

Here, the conjugated variables $\widehat{\theta}$ and $\widehat{n}$ are respectively the difference between the phases across each junction of the transistor, and the number of excess Cooper pairs in this island; $E_C = (2e)^2/(2C_\Sigma)$ is the charging energy of the island with total capacitance C_Σ, and n_g the reduced gate charge in units of $2e$. This hamiltonian is easily diagonalised in the eigenbasis of the charge operator $\widehat{n}$. The eigenstates $|i\rangle$, with energy $E_i(\delta, n_g)$, sustain a supercurrent $I_i = \varphi_0^{-1}(\partial E_i/\partial\delta)$ and correspond to an island voltage $V_i = (2e)^{-1}(\partial E_i/\partial n_g)$. When E_J^0 is not much larger than E_C, and n_g close to $1/2$, the two lowest energy states, labelled 0 and 1 are well separated from the other levels and can be used to implement a qubit. In this circuit, the qubit manipulation can be performed by applying microwave pulses at the qubit transition frequency $\Omega/2\pi = (E_1 - E_0)/h$ on the gate electrode. When E_J^0 is not large compared to E_C, the energies of the qubit levels are well approximated by:

$$E_{0,1} = \mp\sqrt{\left(E_J^0 \cos(\delta/2)\right)^2 + \left(E_C(1 - 2n_g)\right)^2}. \qquad (2)$$

Although the qubit states can be used over a wide parameter range, some biasing points are more attractive. In particular, at the electrostatic energy degeneracy point $n_g = 1/2$, one has $\partial E_i/\partial n_g = 0$, and, at $\delta = 0$, $\partial E_i/\partial\delta = 0$. At the biasing point $(n_g = 1/2, \delta = 0)$, the qubit frequency is set by the Josephson energy of the junctions, and is only affected in second order by fluctuations of the control parameters. Dephasing of the qubit should thus be minimized at this biasing point. In particular, the random offset charge noise [9] should less affect this circuit than the Cooper-pair box [8]. In the proposed set-up, the qubit is maintained at the biasing point $(n_g = 1/2, \delta = 0)$ during its ma-
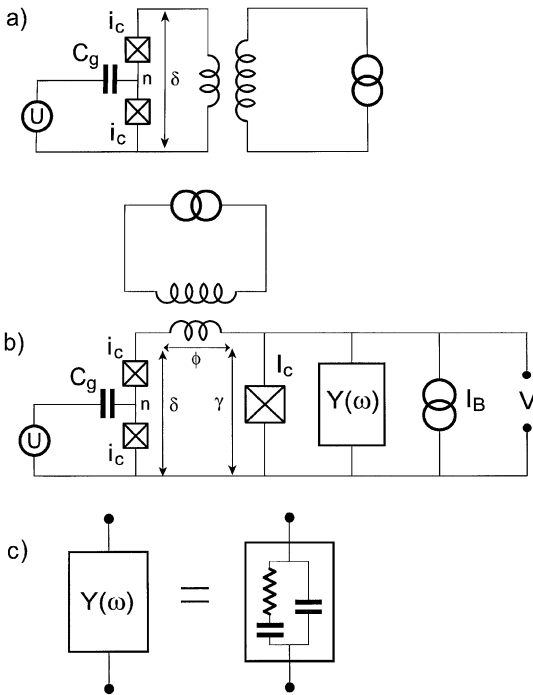
nipulation, and the phase δ is varied only during the readout.

The qubit circuit is shown in Fig. 1b: another Josephson junction, with a Josephson energy $E_J = \varphi_0 I_C \gg E_J^0$, is inserted in the loop in order to readout the qubit. The principle of the readout is based on the dependence on the qubit state i of the critical current I_{Ci} of the parallel combination of the transistor and of the large junction. This critical current is the maximum value of $I_{Ci}(\gamma) = I_C \sin\gamma + I_i(\phi + \gamma)$, where γ is the phase across the readout junction, and $(\phi + \gamma)$ the phase across the SCPT. Because the large junction imposes to a good approximation the phase across the transistor, the critical current almost corresponds to $\gamma = \pi/2$. We demonstrate in the following that the critical current can be determined with sufficient accuracy to discriminate both qubit states.

3. Readout resolution

The determination of the critical current can be performed by detecting the transition to a finite voltage state when the bias-current approaches it. This switching transition is easily detected by monitoring the voltage across the system. The switching out of the zero-voltage state of a current-biased Josephson junction has been thoroughly investigated. The current-biased junction is indeed a model system for the dynamics of a single degree of freedom whose coupling to an environment can be controlled [10,11]. The dynamics of the phase γ is that of a particle with mass $C\varphi_0^2$, placed in a tilted washboard potential $U = -E_J \times (\cos\gamma + s\gamma)$, with $s = I/I_C$, and subject to retarded friction determined by the admittance $Y(\omega)$ of the circuit in parallel with the junction. Below the critical value $s = 1$, the potential has metastable equilibrium positions. The phase dynamics is characterised by the frequency $\omega_P/2\pi$ and the quality factor Q of the oscillations at the bottom of the wells. For s close to 1, the oscillation frequency is

$$\omega_P/2\pi \simeq \left(\frac{\sqrt{2} I_C}{\varphi_0 C_{\text{eff}}} \right)^{1/2} (1 - s)^{1/4}. \tag{3}$$

In this expression, we have assumed that the capacitance C_{eff} includes the eventual contribution of the environment. The quality factor is then $Q = C\omega_P/\text{Re}\,Y(\omega_P)$. For underdamped or moderately damped junctions ($Q \gtrsim 1$), escape out one of these wells triggers the run-away of the phase down the washboard potential, and a finite voltage develops. At high temperature, the phase across the junction is an almost classical variable and switching occurs by thermal activation over the potential energy barrier. The rate of this process follows Kramers' law:

$$\Gamma_{\text{cl}} = a \frac{\omega_P}{2\pi} \exp\left(-\frac{\Delta U}{k_B T} \right), \tag{4}$$

where $\Delta U \simeq (4\sqrt{2}/3)E_J(1 - s)^{3/2}$, and a is a prefactor of order 1 in the regime $Q \approx 1$. Below the cross-over temperature defined by $k_B T_{\text{CO}} = \hbar\omega_P/2\pi$, escape occurs mainly by quantum tunneling "through" the potential energy barrier [11]. For $Q \gtrsim 1$, the quantum rate does not depend on Q and is:

$$\Gamma_q = 52\sqrt{\frac{\Delta U}{\hbar\omega_P}} \frac{\omega_P}{2\pi} \exp\left(-7.2\frac{\Delta U}{\hbar\omega_P} \right). \tag{5}$$

It is useful to define the escape temperature T_{esc} through the relation:

$$\Gamma = \frac{\omega_P}{2\pi} \exp(-\Delta U/k_B T_{\text{esc}}). \tag{6}$$

The theoretical predictions for a junction in the $Q \gtrsim 1$ regime are $T_{\text{esc}} \simeq T$ above the cross-over temperature T_{CO}, and $T_{\text{esc}} \simeq \hbar\omega_P/7.2k_B$ below. Quantum corrections in the thermal activation regime, and thermal corrections in the quantum regime slightly increase the escape temperature above these values.

When a bias-current pulse I is applied during a time τ, the switching probability for each qubit state i is $P_{Si} = 1 - \exp(-\Gamma_i\tau)$. If these probabilities are different enough, switching provides a single-shot measurement of the qubit. We define the discriminating power of the readout system as $\alpha = |P_{S1} - P_{S0}|$. Single-shot readout is achieved when α is close to 1. The relations (4) and (5) show that the discriminating power is determined by thermal and quantum fluctuations, which limit the slope $d\Gamma/dI$.

In order to increase this slope, one should decrease the escape temperature till it reaches the temperature of the experiment, and decrease I_C. Since the quantum escape temperature is set by the readout junction plasma frequency, which is imposed if all junctions are fabricated in the same pump-down, the only way to decrease it significantly is to add an extra capacitance to the readout junction capacitance. Decreasing the critical current I_C is in conflict with the requirement of a good phase bias of the SCPT, and a compromise has to be found, as discussed below. In the present design, the ratio between the readout junction critical current $I_C \approx 1$ μA and the SCPT supercurrent is about 100. Finally, the time resolution is limited by the readout pulse duration, provided that the readout junction stays at thermal equilibration in its potential well when the bias-current is raised. For that purpose, its Q factor should not be too large.

4. Back-action of the environment and of the readout system on the qubit

In fine, the sensitivity of a readout system has to be weighted by its back-action on the qubit during manipulation and readout. As already discussed in the case of the single Cooper-pair box measured by an electrometer [5,12,13], different processes contribute to this back-action. First, the qubit can undergo a transition from the upper state to the ground state by transferring the energy $\hbar\Omega$ to the degrees of freedom it is coupled. This process defines the relaxation time T_R. The reverse excitation process is also possible, and is characterised by an excitation time T_E. Both T_R and T_E are expected to differ when readout is off or on. In particular, T_E is expected to be much longer in the off state, when no energy is available to excite the qubit, than in the on state. When a coherent superposition of qubit states is prepared, it is furthermore randomly dephased by the low frequency fluctuations of the qubit hamiltonian due to both the environment and the measuring system. Dephasing is expected to occur much faster when readout is on because the qubit is no longer decoupled from phase fluctuations.

We first discuss the back-action when readout is off, i.e. at zero-bias-current. In this case, phase fluctuations are small, and the whole circuit connected to the SCPT can be treated as an effective impedance $Z_{eff}(\omega) = (Y(\omega) + jC_{eff}\omega - jI_C/\varphi_0\omega)^{-1}$. Symmetry arguments show that the qubit is not coupled to its environment when the SCPT junctions are balanced, as already mentioned. When SCPT junction asymmetry $d = |E_{J_1}^0 - E_{J_2}^0|/(E_{J_1}^0 + E_{J_2}^0)$ is taken into account, the relaxation time T_R is:

$$T_R \approx \frac{4}{d^2} \frac{\varphi_0}{\text{Re}[Z_{eff}(\Omega)]i_C}, \tag{7}$$

in which we have used Eq. (2). Excitation is negligible ($T_E \gg T_R$), and no dephasing still occurs. Taking into account practical limitations on the junction asymmetry ($d > 0.1$), we estimate $T_R > 20$ μs for the admittance shown in Fig. 1c, and for the parameters $E_J^0 = 2E_C = 0.4k_B$ K. Assuming that the gate charge can be tuned at better than $0.02e$, we estimate that the phase coherence time is limited by the offset charge noise [9] at $T_\varphi > 1$ μs. Note that a duration of 1 μs allows to perform about 100 qubit manipulations.

When readout is on, the phase excursions are not bounded, and only approximate expressions have been obtained. The main result is that the phase coherence time is extremely short $T_\varphi \simeq 50$ ns. This simply means that the readout system has dephased the qubit before the "pointer" has moved. We find that T_E is still longer than $T_R > 10$ μs, which we have calculated by averaging over the phase dynamics, assuming that the readout junction plasma frequency is lower than the qubit transition frequency. Circuit design thus results from a trade-off between efficient readout, long relaxation and dephasing times when readout is off, and weak relaxation/excitation when readout is on.

5. Sample fabrication and experimental set-up

Samples were fabricated by electron-beam lithography in a two-step process. First, an interdigitated 1.0 pF capacitor and small metallic

islands, made out of gold, were deposited. The role of the capacitor is to decrease the readout junction resonance frequency in order to improve the discriminating power, while that of the metallic islands is to provide a normal metal sink for spurious quasiparticles in the SCPT electrodes [7]. It is indeed essential to avoid a single quasiparticle entering the SCPT island, which would destroy the desired qubit states at $n_g = 1/2$. In a second step, the SCPT and the readout junction were fabricated by depositing aluminum layers at two angles through a suspended shadow-mask [14]. The first layer was oxidized in order to grow the tunnel junction barriers. Similar SCPT and readout junction are fabricated together with the qubit circuit for the sake of tunnel resistance control. The sample was wire-bonded onto a miniature circuit-board with surface mounted components. The board was fitted in a shielded copper box thermally anchored to the mixing chamber of a dilution refrigerator. All lines were carefully filtered [15] in order to reach thermal equilibrium at the base temperature 14 mK. The bandwidth of the current-biasing line was however kept large enough to pass submicrosecond readout square pulses. When switching occurs, the voltage on the measuring line with capacitance $C_M \approx 0.5$ nF rises at a rate $I_C/C_M \approx 1$ mV/µs. The switching was detected by monitoring the voltage across the readout junction using a low-noise amplifier with a 1 MHz bandwidth.

6. Experimental results

We report here switching experiments in a sample with the SCPT disconnected on purpose. We have measured the switching rate of the readout junction alone as a function of bias-current and temperature, using square pulses with adjustable height, or linear ramps [16] for current-biasing the readout junction. The variations of the switching probability when the height of 0.5 µs readout pulses is varied are shown in Fig. 2 for different temperatures. The maximum slope, obtained at the lowest temperature, would correspond to a discriminating power of 0.6 for the readout. Switching rates obtained using both
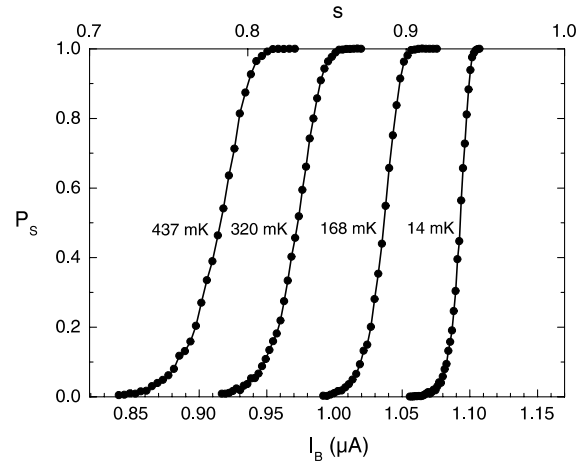

Fig. 2. Switching probability P_S of the readout junction when 0.5 µs long bias-current square pulses with variable amplitude are applied. The critical current is $I_C = 1.17$ µA. The steepest step, obtained at the lowest temperature, would correspond to a discriminating power of 0.6 in a single shot readout of the qubit.
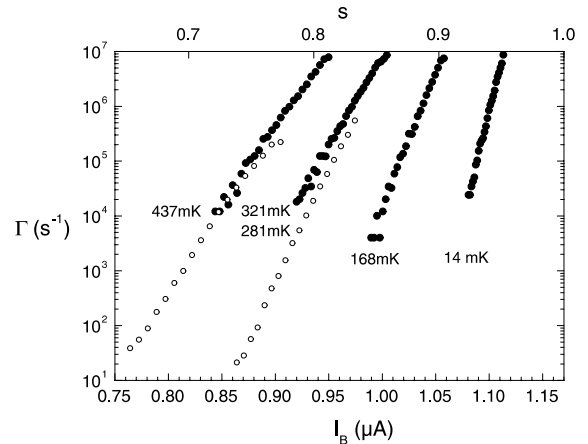

Fig. 3. Switching rate of the readout junction as a function of bias-current $I_B = sI_C$ at different temperatures. Full symbols correspond to 0.5 µs long bias-current square pulses, and open symbols to linear bias-current ramps at $dI_B/dt = 0.84$ µA/ms.

measurement techniques are shown in Fig. 3 as a function of bias-current, for different temperatures. The escape temperature defined by Eq. (6), and determined following the procedure described in Ref. [17], is plotted in Fig. 4. The lowest measured escape temperature is about 90 mK, which is
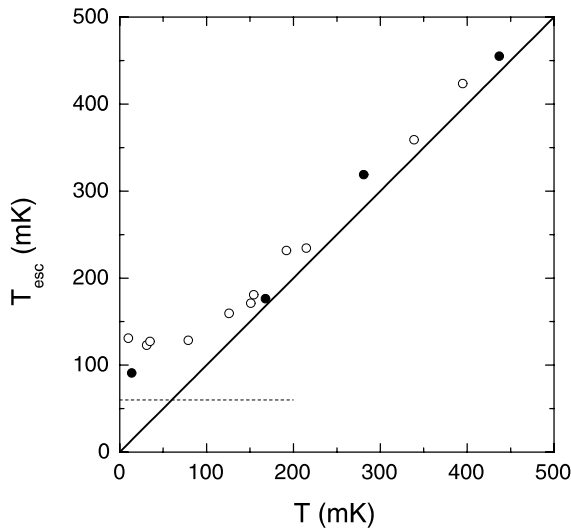
Fig. 4. Escape temperature versus sample temperature. Full symbols correspond to bias-current square pulses, and open symbols to linear bias-current ramps. We attribute the difference found at low temperature between both methods to the larger heating of the damping circuit when linear ramps are used. The dashed line indicates the predicted escape temperature assuming that the on-chip capacitance fully adds to the junction capacitance, and that no spurious heating occurs.

higher than the design value of 60 mK predicted using Eq. (5), assuming that the on-chip capacitor fully contributes to the capacitance C_{eff}. We attribute this discrepancy to two effects. First, the SMC resistor in the bias-current line is slightly heated by the bias-current, as indicated by the increase observed when relatively slow bias-current ramps are used instead of fast pulses. Second, the on-chip added capacitance is not fully effective because of the residual inductance of the connecting lines and of the capacitance itself. Quantitatively, we have calculated that the quantum tunneling rate is the same as if about half of the on-chip capacitance was effectively contributing [18]. These two effects explain well the value of the minimum escape temperature, and of the resulting discriminating power. These results, which already allow interesting measurements on the qubit to be performed, can be improved, and a discriminating power of 0.95 with 200 ns long readout pulses could be achieved if the predicted escape temperature of 60 mK is reached.

7. Conclusions

We have discussed a new design for a combined charge-phase qubit, based on a SCPT connected in parallel with a large readout junction. Whereas the qubit is addressed using the gate charge coupled to the transistor island, the readout is performed using the supercurrent driven by the phase difference across the transistor, which controls the switching of the readout junction out of the zero-voltage state. From measurements of the switching probability of this junction when a square bias-current pulse is applied, we have determined the discriminating power of the readout. We conclude that single-shot measurements should be possible in this system. Experiments on a full qubit circuit are in progress.

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